New Piezoelectric Transformer Adapter with Universal Input Voltage Range

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***Abstract*—For the design of the AC-DC PT (Piezoelectric Transformer) adapter with a universal input voltage, it is important not only to find a solution to cover the wide range of input voltages but also to maintain control in the narrow switching frequency range. In general, PT efficiency is maximal near the peak gain point under the optimal load. As the operating frequency moves away from the peak gain point, the PT efficiency decreases due to the increase of the circulating current. In the half-bridge type circuit, which is widely used to implement an AC/DC PT adapter using PFM(Pulse Frequency Modulation), the above-mentioned problem exists if the universal input voltage specification is required. In this paper, a new circuit topology and control scheme for an AC-DC adapter with a universal input voltage range is proposed. Compared to the conventional half-bridge type, the proposed circuit has the following advantage. The range of the operating switching frequency is very narrow in spite of the universal input voltage variation(ac 90~250Vrms) because the switch S1 with PWM control for line regulation and the switch S2 with PFM control for load regulation operate almost independently. Thus, the proposed circuit has a uniform efficiency over the universal input voltage which is higher than the half-bridge type. Based on the analysis, as well as the simulation and experimental results provided in this paper, it is confirmed that the proposed circuit can be a good solution for the universal off-line input voltage specification.**

Keywords-Piezoelectric Transformer; adapter;Universal input voltage; PWM;PFM

I. INTRODUCTION

Due to its many advantages in comparison with magnetic transformers, such as low profile, high power density, no winding suitable to automated manufacturing, high degree of insulation, and no electromagnetic noise, a piezoelectric transformer can be an attractive solution for AC-DC adapter applications[1]-[5].

For the design of the PT adapter with a universal input voltage, it is important not only to find a solution to cover the wide range of input voltages but also to maintain control in the narrow switching frequency range. In general, PT efficiency is maximum near the peak gain point under the optimal load. As the operating frequency moves away from the peak gain point, the PT efficiency decreases due to the increase of the circulating current. In the half-bridge type circuit, which is widely used to implement an AC/DC PT adapter using PFM(Pulse Frequency Modulation), as shown in Fig. 1, the above-mentioned problem exists if the universal input voltage specification is required. Especially, at the high-line input voltage the operating switching frequency is the furthest from the desired point, thus resulting in a decrease in efficiency.

In this paper, a new circuit topology and control scheme for an AC-DC adapter with a universal input voltage range is proposed as shown in Fig.2. Compared to the conventional half-bridge type, the proposed circuit has several advantages. First, the range of the operating switching frequency is very narrow in spite of the universal input voltage variation(ac 90~250Vrms) because the switch S_1 with PWM control for line regulation and the switch S_2 with PFM control for load regulation operate almost independently. Thus, the proposed circuit has a uniform efficiency over the universal input voltage which is higher than the half-bridge type. Second, the overall component of the power stage is the same as the half-bridge inverter except one additional diode, D_1.

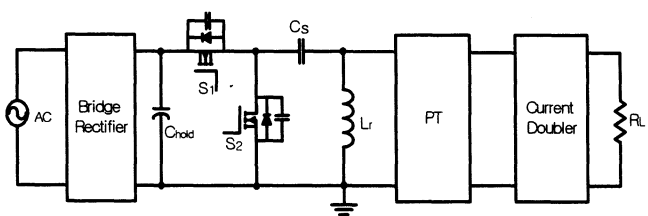


Figure 1. Half-bridge type PT adapter

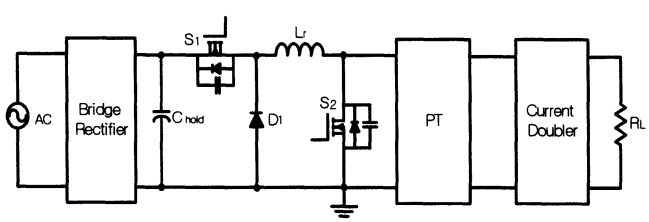


Figure 2. New circuit topology for the PT adapter

A detailed analysis of the proposed converter is carried out using an equivalent circuit of the piezoelectric transformer.

These analytical results are verified by experiments. As a result, good regulation for both line and load variations is successfully achieved. As compared with the half-bridge type inverter, it is confirmed that the proposed circuit over the universal input voltage has a nearly constant efficiency, which is higher than the half-bridge type. Experimental results of a 7.2W prototype hardware yielded an efficiency of 70~76% at an input voltage of ac 90~250Vrms, an output voltage of 12V, and a load current of up to 0.6A.

II. Structure and Characteristics of Piezoelectric Transformer

Figure 3 shows the structure and dimension of the disk-type PT sample operating in the radial mode. The fundamental resonant frequency is around 151 kHz, the primary electrode is placed in the center, and the secondary electrode consists of 3 layers. An electrical equivalent circuit of the PT is presented in Fig.4. These parameters are calculated by measuring the electrical characteristics of the PT using the network analyzer HP4194A. The voltage gain and the efficiency of the PT itself are measured experimentally, as shown in Fig.5. The maximum efficiency is in the vicinity of the peak gain frequency.

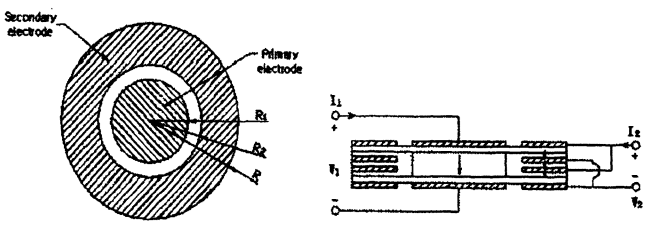
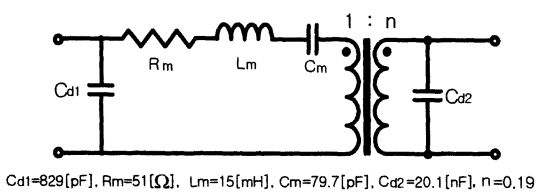
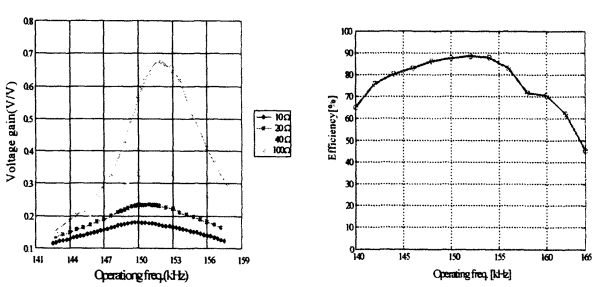


Figure 3. Structure and dimension of the radial-mode disk-type PT



Cd1=829[pF], Rm=51[Ω], Lm=15[mH], Cm=79.7[pF], Cd2=20.1[nF], n=0.19

Figure 4. Equivalent circuit model of the disk-type PT



(a) Voltage gain (b) Efficiency (R_L =20Ω)

Figure 5. Characteristics of the disk-type PT with load resistance R_L (Condition: Input voltage of PT is power level)

III. The Proposed Circuit Configuration and Operation

A. Circuit Operation

As shown in Fig.2, the proposed circuit is cascaded by a buck converter and a class-E inverter. It is noteworthy that the inductance, Lr, acts not only as an output filter of the buck converter when S_1 and S_2 are on, but also as the resonant inductor of the class-E inverter when S_2 is off. In addition, the output rectifier serves as a current doubler circuit. The subsequent analysis is performed under the following assumptions:

- The minimum loaded quality factor is high enough so that the current through the L_m-C_m branch, that is, I_m is approximately a sine wave.
- The components of the converter are ideal.
- The input voltage which is rectified by the input bridge diode and the hold capacitor (C_{hold}) voltage is regarded as a constant voltage source.
- The MOSFET switches S_1 and S_2 operate at the same frequency, and turn on at the same time. S_2 has a fixed 50% duty ratio and operates above resonance for zero voltage switching (ZVS).
- The inductance, Lm, of the PT is assumed to be high enough so that C_{in} resonates with L_r at the operating frequency.
- The output filter inductor is large enough so that its current is regarded as a DC current source Io/2.

Base on the above assumptions, the simplified circuit is obtained as shown in Fig.6.

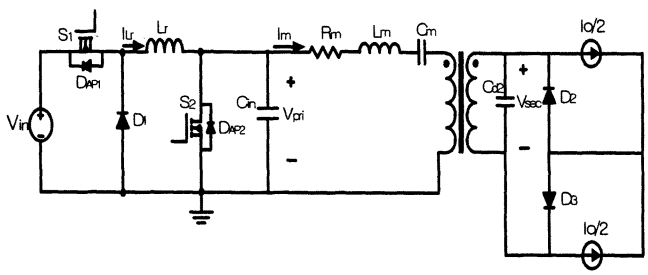
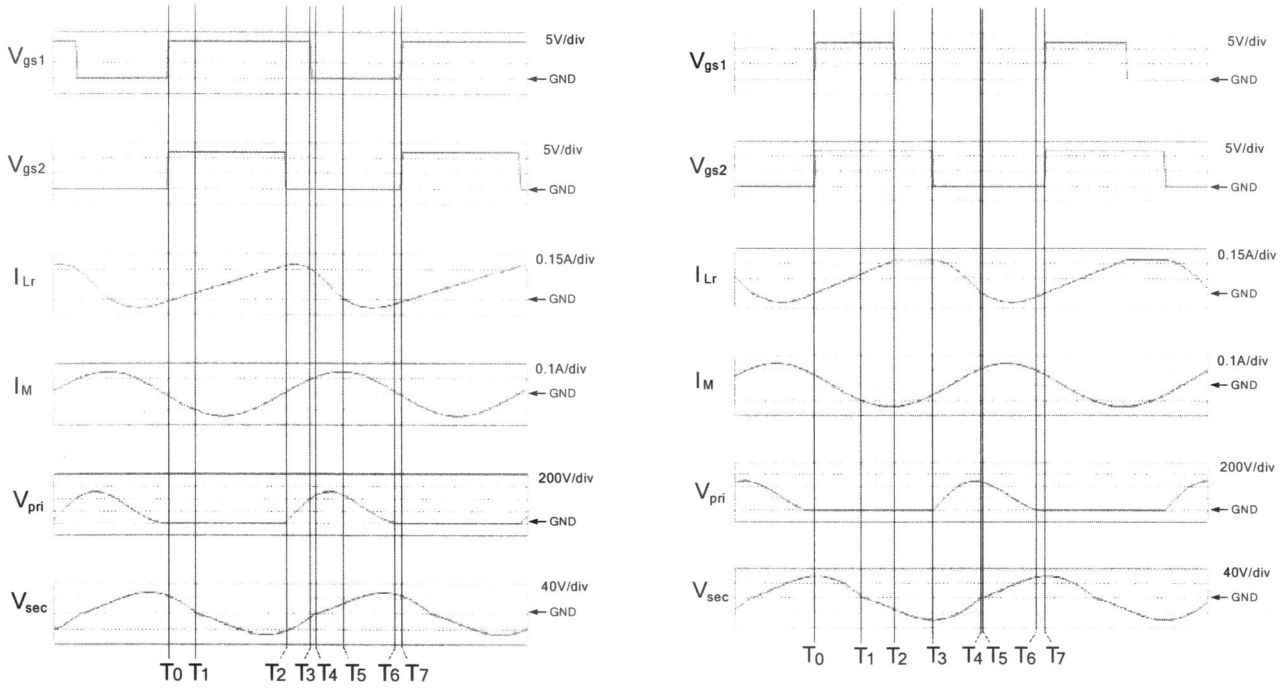


Figure 6. Simplified equivalent circuit of the proposed PT adapter

B. Operation Mode Analysis

The operation of the proposed circuit has two parts according to whether the duty ratio of switch S1 is smaller or larger than that of switch S2, that is, D1 ≥ D2 (Case I) and D1 < D2 (Case II). Both Case-I and Case-II have seven operation modes during one switching cycle. The simulated key waveforms and the equivalent circuit of each operation mode are shown in Fig. 7 and 8, respectively. All operation modes except for mode-3 and mode-4 are common.



(a) Case I (D1 ≥ D2)

(b) Case II (D1 < D2)

Figure 7. Key waveforms of the proposed circuit (Vgs1 and Vgs2 is the gate-to-source voltage of the switches S1 and S2, respectively. ILr is the current through Lr. IM is the current through the branch of Lm-Cm. Vpri and Vsec is the voltage of PT primary-side and PT secondary-side, respectively.)

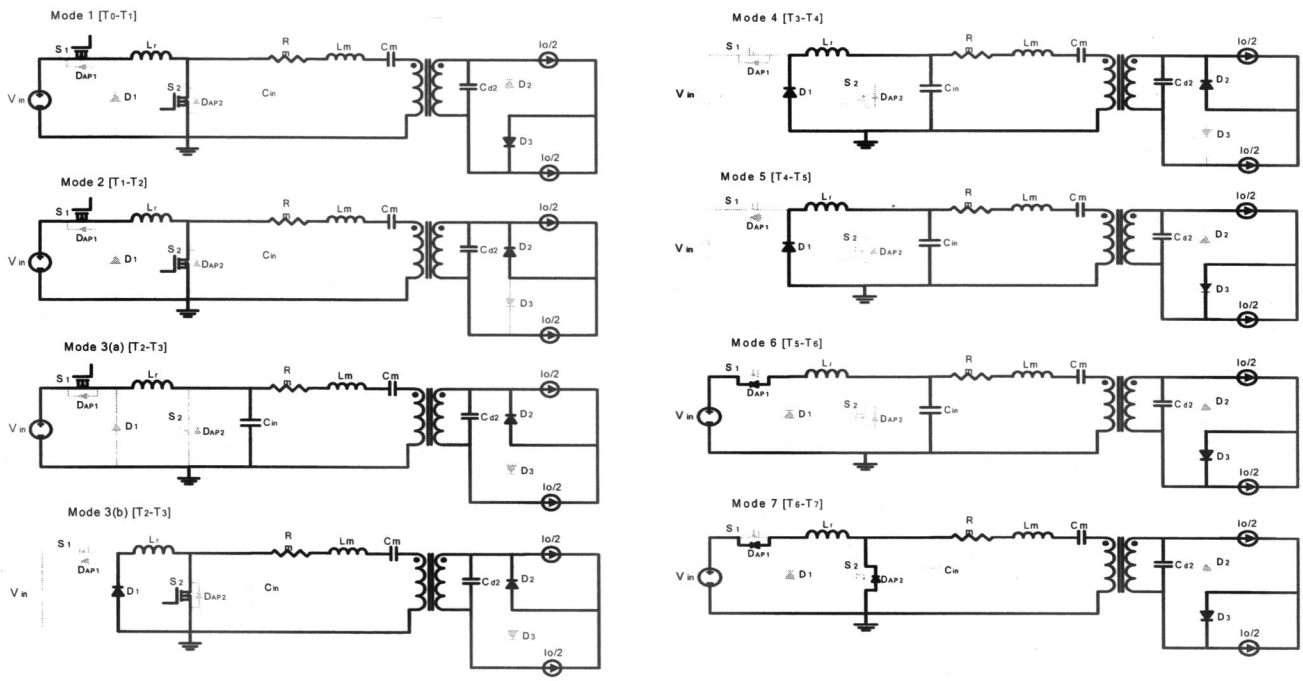


Figure 8. Operation modes (All modes except for Mode 3 have the same circuit configuration. Mode 3(a) for D1 ≥ D2 , Mode 3(b) for D1 < D2. In other words, the modes for D1 ≥ D2 are [1]-[2]-[3(a)]-[4]-[5]-[6]-[7], and those for D1 > D2 are [1]-[2]-[3(b)]-[4]-[5]-[6]-[7].

Mode-1 [T_0-T_1]: The current I_{S2} is negative prior to T_0, so the current flows through the antiparallel diode of the switch S_2. At T_0, S_1 and S_2 turn on at the same time, and S_2 operates at zero voltage switching(ZVS). The current through L_r linearly increases until S_1 turns off.

Mode-2 [T_1-T_2]: At T_1, the PT secondary voltage is zero crossing and decreases, so D_2 turns on and D_3 is off.

Mode-3(a) [T_2-T_3]: This mode exsits in Case-I. At T_2, S2 turns off. The energy of L_r stored during mode 2 is discharged through the capacitor Cin, and the voltage across C_{in} is increased.

Mode-3(b) [T_2-T_3]: This mode exsits in Case-II. At T_2, S1 turns off. Because D_1 is conducted by I_{Lr}, the stored energy of L_r is circulated through the path formed by D_1, Lr, and S_2. The PT primary voltage is still zero.

Mode-4 [T_3-T_4]: In Case-I, S_1 turns off at T_3, and D_1 is on at the same time. C_{in} is continueouly charged by the resonance with L_r until Vpri reaches zero. On the other hand, in Case-II, S_2 turns off at T_3. C_{in} begins to be charged in the same manner as Case-I.

Mode-5 [T_4-T_5]: At T_4, the PT secondary voltage is zero crossing and increases, so D2 turns off and D1 is on.

Mode-6 [T_5-T_6]: At T_5, the current through Lr is zero crossing, and the antiparallel diode of S_1 (D_{AP1}) is conducted.

Mode-7 [T_6-T_7]: At T_6, the PT primary voltage reaches zero and the anti-parallel diode of S_2 (D_{AP2}) is conducted. At T_7, S_1 and S_2 turn on and the next cycle begins.

IV. CONTROL SCHEME

The switch S_1 with PWM control for line regulation and the switch S_2 with PFM control for load regulation operate almost independently. It is easy to design and implement the feedback circuit as shown in Fig.9. That is, the peak input voltage of the PT primary input voltage is regulated by PWM control using a peak detector as shown in Fig.9(a). Figure 9(b) shows the block diagram for the output voltage feedback circuit.

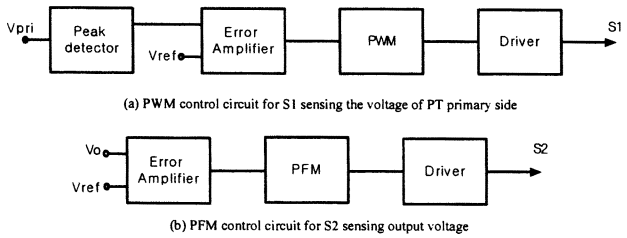


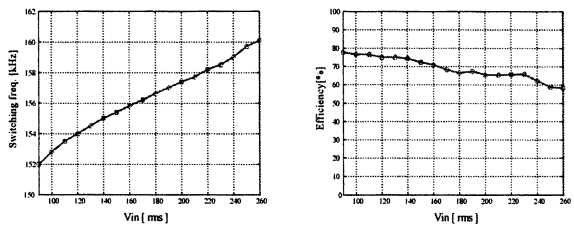
Figure 9. Block diagram of feedback control circuit

V. EXPERIMENTAL RESULTS

Experiments of both the conventional half-bridge type circuit and the proposed circuit for the same condition are carried out. The specifications are as follows: The input voltage (Vin) is ac 90~250Vrms, the output voltage (Vo) is 12V, and the maximum output current is 0.6A. (R_L=20Ω)

A. Conventional half-bridge type cirucit

The detailed circuit component values of the hardware are shown in Table I. Figure 10 shows the operating switching frequency and the overall measured efficiency of the half-bridge type circuit. The overall circuit efficiency decreases from 77% to 60% as the input voltage increases.

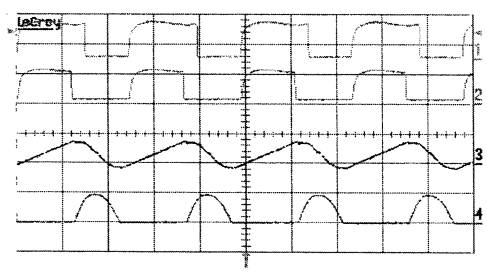


(a) Switching frequency fs (b) Measured efficiency

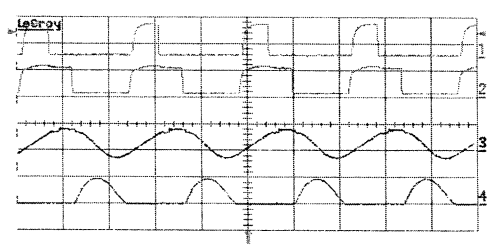
Figure 10. Operating switching frequency fs and overall measured efficiency of half-bridge type

B. Proposed circuit

The detailed circuit component values of the hardware are shown in Table II, and implemented with the prototype hardware. Figure 11 shows the hardware waveforms. The waveforms are the same as the simulation results as shown in Fig.7.



(a) Vin = 110Vrms, fs=152.5kHz, D1=0.6



(b) Vin = 230Vrms, fs=152.5 kHz, D1=0.18

Figure 11. Experimental waveforms(Ch1; Switch S1 gate signal [10V/div], Ch2: Switch S2 gate signal [10V/div], Ch3: Inductor Lr current [0.5A/div], Ch4: PT primary voltage[400V/div])

TABLE I. COMPONENTS VALUE OF HALF-BRIDGE TYPE

Components	Parameters
L_r	EPC25B, 0.5mH
L_1, L_2	EPC17, 0.3mH
C_O	220uF/25V
S_1,S_2	IRF830 (500V, 4.5A)
C_S	100nF/630V ceramic
D_2,D_3	MBRS1100(100V, 1A)

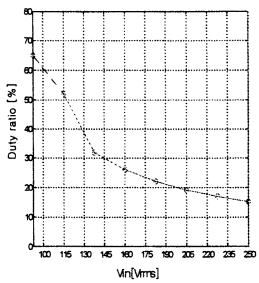
TABLE II. COMPONENTS VALUE OF THE PROPOSED CIRCUIT

Components	Parameters
L_r	EPC25B, 0.65mH
L_1, L_2	EPC17, 0.3mH
C_O	220uF/25V
S_1,S_2	IRF830 (500V, 4.5A)
D_1	UF5406 (600V, 3A)
D_2,D_3	MBRS1100(100V, 1A)

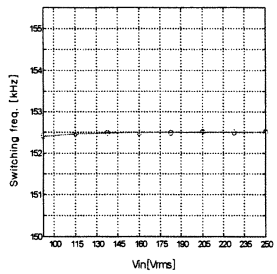
Figure 12(a),(b) shows the measured results of the duty ratio D_1 of switch S1 and the switching frequency, fs, as a function of the input voltage. The switching frequency, fs, is nearly constant for the regulation of the PT primary voltage and the output voltage. Figure 12(c) shows the measured efficiency of the PT adapter. The efficiency is nearly constant over the universal input range.

VI. CONCLUSION

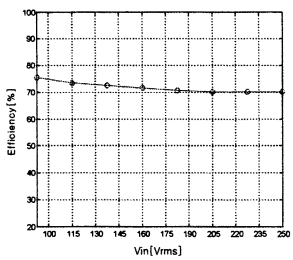
A new PT adapter topology which has a narrow switching frequency range for the universal input voltage range is proposed. The proposed circuit is compared to the half-bridge type circuit, which has a wide switching frequency range. Maintaining the operating frequency in a narrow range in the vicinity of the peak PT gain frequency results in a higher efficiency of the PT. In this view point, the proposed circuit is desirable. Experimental results show a nearly constant efficiency of 70~76%, which is higher than the half-bridge type at an input voltage of ac 90~250Vrms, an output voltage of 12V, and a load current up to 0.6A. Based on the analysis, as well as the simulation and experimental results provided in this paper, it is confirmed that the proposed circuit can be a good solution for the universal off-line input voltage specification.



(a) Duty ratio D1



(b) Switching frequency fs



(c) Measured efficiency

Figure 12. Measured duty ratio D_1 of the switch S_1, operating frequency fs of the switch S_2, and measured efficiency

REFERENCES

[1] C. A. Rosen, "Ceramic Transformer and Filters," Proc. Electronic Comp. Symp., pp.205 –211, 1956

[2] T. Zaitsu, Y. Fuda, Y. Okabe, T. Ninomiya, S. Hamamura, and M. Katsuno, "New Piezoelectric Transformer Converter for AC-adaptor," IEEE APEC, pp. 568-572, 1997.

[3] Sungjin Choi, Taeil Kim and Bo. H. Cho, "Design of Half-Bridge Piezo-Transformer Converters in the AC Adapter Applications," IEEE APEC, pp. 244-248, 2005.

[4] S. Hamamura, T. Ninomiya, M. Yamamoto, and M. Katsuno, "Combined PWM and PFM Control for Universal Line Voltage of a Piezoelectric Transformer Off-Line Converter," IEEE Transaction on Power Electronics, vol. 38, No. 1, Jan 2003.

[5] Yunxiu Li, and Wei Chen, "AC-DC converter with Worldwide Range Input Voltage by Series and Parallel Piezoelectric Transformer Connection," IEEE PESC, pp. 2668-2671, 2004.